# CLAIMS

WHAT IS CLAIMED:

1. An apparatus for testing a memory device having a plurality of data lines, comprising:

an input circuit adapted to receive at least a first subset of the data lines and a plurality of enable signals, each enable signal being associated with at least one of the first subset of data lines;

a compression circuit coupled to the input circuit and being adapted to detect a predetermined pattern on the first subset of data lines; and

an output circuit coupled to the compression circuit and adapted to provide at least a pass signal when the predetermined pattern is detected on the first subset of data lines, wherein the input circuit is capable of masking at least one of the first subset of data lines from the compression circuit based on the associated enable signal.

2. The apparatus of claim 1, wherein the input circuit comprises:

a multiplexer having an input coupled to a first data line of the first subset of data lines, a first control input coupled to receive a first enable signal associated with the first data line, and an output;

a transistor coupled between the output of the multiplexer and a voltage source and having a base input coupled to receive the first enable signal.

3. The apparatus of claim 2, wherein the voltage source is a positive voltage source.

4. The apparatus of claim 3, wherein the multiplexer includes a second control input, and the input circuit further includes an inverter coupled to the first enable signal and the second control input.

5. The apparatus of claim 2, wherein the voltage source is ground and the input circuit further includes an inverter coupled between the first enable signal and the transistor.

6. The apparatus of claim 5, wherein the multiplexer includes a second control input and the inverter is coupled to the second control input.

7. The apparatus of claim 3 wherein the compression circuit is adapted to perform a NAND Boolean function.

8. The apparatus of claim 5 wherein the compression circuit is adapted to perform a NOR Boolean function.

9. The apparatus of claim 1, wherein the plurality of data lines include a second subset of data lines having a first data topology and a third subset of data lines having a second data topology, and the second subset is interleaved with the third subset.

10. An apparatus for testing a memory device having a plurality of data lines, comprising:

an input circuit including a latch, the latch being coupled to at least a first subset of the data lines;

a compression circuit coupled to the latch and being adapted to detect a predetermined pattern on the first subset of data lines; and

an output circuit coupled to the compression circuit and adapted to provide at least a pass signal when the predetermined pattern is detected on the first subset of data lines.

11. The apparatus of claim 10, wherein the input circuit includes a first logic gate adapted to receive a latch signal and a clock signal and to enable the latch based on a first combination of the latch signal and the clock signal.

12. The apparatus of claim 11, wherein the latch includes a first multiplexer having a first multiplexer input coupled to a first data line of the first subset of data lines, a first control input coupled to the first logic gate, and a first multiplexer output.

13. The apparatus of claim 12, wherein the latch further comprises:

a first inverter having a first inverter input coupled to the first multiplexer output, and a first inverter output; and

a second inverter having a second inverter input coupled to the first inverter output and a second inverter output coupled to the first inverter input.

14. The apparatus of claim 13, wherein the latch further comprises a second multiplexer having a second multiplexer input coupled to the first inverter output, and a second multiplexer output.

15. The apparatus of claim 14, wherein the input circuit includes at least a second logic gate adapted to receive the latch signal and the clock signal and to enable the second multiplexer based on a second combination of the latch signal and the clock signal.

16. The apparatus of claim 14, wherein the latch further comprises:

a third inverter having a third inverter input coupled to the second multiplexer output, and a third inverter output; and

a fourth inverter having a fourth inverter input coupled to the third inverter output and a fourth inverter output coupled to the third inverter input.

17. The apparatus of claim 16, wherein the third inverter output is coupled to the compression circuit.

18. The apparatus of claim 10, wherein the input circuit is adapted to receive a plurality of enable signals, each enable signal is associated with one of the first subset of data lines, and the input circuit is capable of masking at least one of the first subset of data lines from the compression circuit based on an associated enable signal.

19. The apparatus of claim 18, wherein the latch includes a latch output and the input circuit further comprises a transistor coupled between the latch output and a voltage source and having a gate coupled to receive the associated enable signal.

20. The apparatus of claim 19, wherein the voltage source is a positive voltage source.

21. The apparatus of claim 19, wherein the voltage source is ground.

22. The apparatus of claim 10 wherein the compression circuit is adapted to perform a NAND Boolean function.

23. The apparatus of claim 10 wherein the compression circuit is adapted to perform a NOR Boolean function.

24. The apparatus of claim 10, wherein the plurality of data lines include a second subset of data lines having a first data topology and a third subset of data lines having a second data topology, and the second subset is interleaved with the third subset.

25. An electronic device, comprising:

a memory core having a plurality of data lines;

a data latch coupled to the memory core and adapted to receive at least a first subset of the plurality of data lines and provide a plurality of latched data lines; and

a compression circuit coupled to the latch and adapted to receive at least a second subset of the latched data lines and detect a predetermined pattern present on the second subset of latched data lines.

26. The electronic device of claim 25, further comprising at least one output pad coupled to the compression circuit.

27. The electronic device of claim 25, wherein the compression circuit includes an input circuit, the input circuit being adapted to receive the second subset of latched data lines and a plurality of enable signals, each enable signal being associated with one of the second subset of latched data lines, wherein the input circuit is capable of masking at least one of the second subset of latched data lines from the compression circuit based on the associated enable signal.

28. The electronic device of claim 25, wherein the plurality of data lines include a third subset of data lines having a first data topology and a fourth subset of data lines having a second data topology, and the third subset is interleaved with the fourth subset.

29. An electronic device, comprising:

a first memory core having a first plurality of data lines;

a second memory core having a second plurality of data lines; and

a compression circuit coupled to the first and second memory cores and adapted to receive at least a first subset of the first plurality of data lines and a second subset of the second plurality of data lines and to detect a predetermined pattern present on one of the first subset and the second subset.

30. The memory device of claim 29, wherein the compression circuit includes an input circuit adapted to receive the first and second subsets and a plurality of enable signals, each enable signal being associated with one data line of the first and second subsets, wherein the input circuit is capable of masking at least one data line of the first and second subsets from the compression circuit based on the associated enable signal.

31. A method for testing a memory device having a plurality of data lines, comprising:

reading data present on at least a subset of the plurality of data lines;

masking the data associated with at least one data line of the subset;

determining if the data matches a predetermined pattern; and

providing at least a pass signal if the data matches the predetermined pattern.

32. The method of claim 31, wherein the determining comprises compressing the data to determine if each datum of the data matches a predetermined value.

33. The method of claim 31, further comprising latching the data present on the subset of data lines.

34. The method of claim 33, wherein the latching is performed prior to determining if the data matches the predetermined pattern.

35. A method for testing a memory device having a plurality of data lines, comprising:

reading data present on at least a subset of the plurality of data lines;

latching the data present on the subset of data lines to provide latched data;

determining if the latched data matches a predetermined pattern; and

providing at least a pass signal if the data matches the predetermined pattern.

36. The method of claim 35, wherein the determining comprises compressing the latched data to determine if each datum of the latched data matches a predetermined value.

37. An apparatus for testing a memory device having a plurality of data lines, comprising:

means for reading data present on at least a subset of the plurality of data lines;

means for masking the data associated with at least one data line of the subset;

means for determining if the data matches a predetermined pattern; and

means for providing at least a pass signal if the data matches the predetermined pattern.

38. An apparatus for testing a memory device having a plurality of data lines, comprising:

means for reading data present on at least a subset of the plurality of data lines;

means for masking the data associated with at least one data line of the subset;

means for determining if the data matches a predetermined pattern; and

means for providing at least a pass signal if the data matches the predetermined pattern.